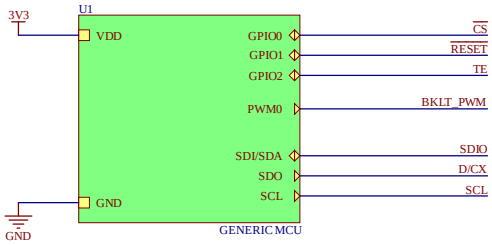
REVISION HISTORY		
REV	DESCRIPTION	DATE
A1	INITIAL RELEASE	20230803

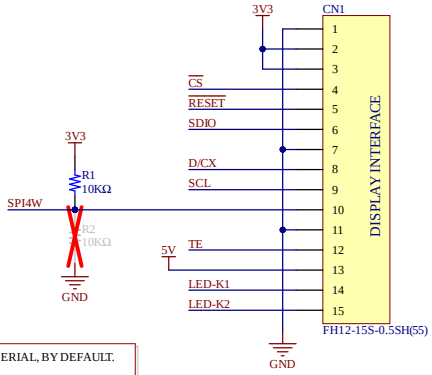
DISPLAYTECH REFERENCE DESIGN

DT018BTFT & DT018BTFT-SHB
(SERIAL CONFIGURATION AND IMAGE DATA)

SERIAL DATA SIGNALS ARE NOT FULLY COMPATIBLE WITH STANDARD SPI DATA PROTOCOLS. CUSTOM DRIVERS ARE NEEDED TO USE SPI HARDWARE PORTS.

A BIT-BANGED IMPLEMENTATION IS AVAILABLE IN THE SAMPLE DRIVER CODE.





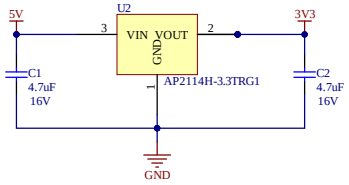
DISPLAY IMAGE DATA IS WRITTEN TO THE DISPLAY DRIVER GRAPHICS RAM (GRAM) VIA THE SERIAL INTERFACE.

ILI9163 DISPLAY DRIVER MUST BE CONFIGURED TO GENERATE FRAME RATE SIGNALS INTERNALLY.

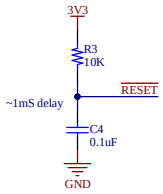
DT018BTFT COMMUNICATION INTERFACE IS (8-BIT) 3-WIRE SERIAL, BY DEFAULT.

FOR 4-WIRE SERIAL COMMUNICATION: POPULATE R1, DE-POPULATE R2.

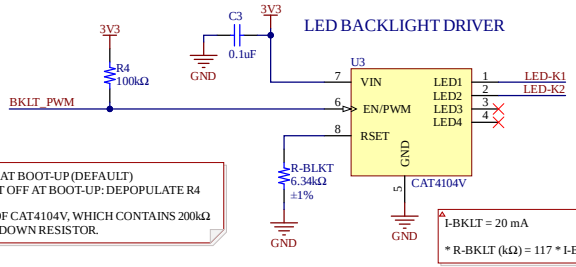
DISPLAY LOGIC POWER



RESET TIMING



LED BACKLIGHT DRIVER



- BACKLIGHT ON AT BOOT-UP (DEFAULT)
- FOR BACKLIGHT OFF AT BOOT-UP: DEPOPULATE R4

*ASSUMES USE OF CAT4104V, WHICH CONTAINS 200kΩ INTERNAL PULL-DOWN RESISTOR.

I-BKLT = 20 mA

* R-BKLT (kΩ) = 117 * I-BKLT ^ (-.978) + 0.05

Project: DT018BTFT & DT018BTFT-SHB			Displaytech a seacomp company
Description: 1.8" SPI RGB LCD		Revision: A1	
Document: Schematic, Reference Design		Sheet Size: A3	Date: 8/10/2023
Drawn: PRW	Approved: JP	Sheet: 1 of 1	Time: 10:44:01 AM
File: G:\Shared drives\US Engineering\2 Displaytech\1 - LCD Modules\IPS & TFT\1.8 inch\DT018BTFT\3 E-CAD\DT			DISPLAYTECH 1525 Faraday Ave., Ste. 200 Carlsbad, CA, 92008